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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,179	01/23/2004	Hiroaki Murakami	SUZU1270	7863
25094	7590 06/28/2005		EXAM	INER
	RUDNICK GRAY CAR	CHANG, DANIEL D		
2000 Universi E. Palo Alto.	ty Avenue CA 94303-2248		ART UNIT PAPER NUMBER	
,	,		2819	
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DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

			DK				
	Application No.	Applicant(s)					
	10/764,179	MURAKAMI ET AI	L.				
Office Action Summary	Examiner	Art Unit					
	Daniel D. Chang	2819					
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply							
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply - If NO period for reply is specified above, the maximum statutory period v - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a reply be ting within the statutory minimum of thirty (30) day will apply and will expire SIX (6) MONTHS from a cause the application to become ABANDONE	nely filed s will be considered timely the mailing date of this co D (35 U.S.C. § 133).					
Status							
1) Responsive to communication(s) filed on 23 Ja	anuary 2004.						
<i>,</i>	action is non-final.						
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is							
closed in accordance with the practice under E	x parte Quayle, 1935 C.D. 11, 4:	53 O.G. 213.					
Disposition of Claims <sup>,</sup>							
<ul> <li>4)  Claim(s) 1-20 is/are pending in the application.</li> <li>4a) Of the above claim(s) is/are withdray</li> <li>5)  Claim(s) is/are allowed.</li> <li>6)  Claim(s) 1,3,5-11,13 and 15-20 is/are rejected.</li> <li>7)  Claim(s) 2,4,12 and 14 is/are objected to.</li> <li>8)  Claim(s) are subject to restriction and/o</li> </ul>	wn from consideration.						
Application Papers	·						
<ul> <li>9) The specification is objected to by the Examine</li> <li>10) The drawing(s) filed on 23 January 2004 is/are: Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct </li> <li>11) The oath or declaration is objected to by the Examine</li> </ul>	a)⊠ accepted or b)⊡ objected drawing(s) be held in abeyance. See ion is required if the drawing(s) is obj	e 37 CFR 1.85(a). jected to. See 37 CF	FR 1.121(d).				
Priority under 35 U.S.C. § 119							
a) All b) Some * c) None of:  1. Certified copies of the priority documents 2. Certified copies of the priority documents 3. Copies of the certified copies of the priority documents application from the International Bureau * See the attached detailed Office action for a list	s have been received. s have been received in Applicati rity documents have been receive u (PCT Rule 17.2(a)).	on No ed in this National	Stage				
Attachment(s)	<i>"</i> □	(DTO 455)					
Notice of References Cited (PTO-892)  Notice of Draftsperson's Patent Drawing Review (PTO-948)	4)						
B) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	5) ☐ Notice of Informal P 6) ☐ Other:		)-152)				

## Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 3, 5-11, 13, and 15-20 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Admitted Prior Art ("AAPA" hereinafter).

Regarding claim 1, AAPA disclose, at least in Fig. 5, a system comprising:

a first logic circuit (510) configured to receive one or more logic circuit input signals (Bin, Ain) and to generate a logic circuit output signal (xor out); and

a multiplexer (520) configured to receive the logic circuit output signal (xor\_out) and one or more additional signals (C) as multiplexer input signals, wherein the multiplexer is configured to receive a select signal (sel, sel\_b) that controls the multiplexer to select one of the multiplexer input signals to be provided as a multiplexer output signal;

wherein when the select signal controls the multiplexer to select the logic circuit output signal as the multiplexer output signal, the first circuit operates in a first mode (logic circuit selected mode), and when the select signal controls the multiplexer to deselect the logic circuit output signal as the multiplexer output signal, the first circuit operates in a second mode (logic circuit deselected mode).

Regarding claim 3, AAPA disclose, at least in Fig. 5, that when the first logic circuit operates in the second mode, the logic circuit output signal contains fewer data transitions than

Application/Control Number: 10/764,179

Art Unit: 2819

when the first logic circuit operates in the first mode (when there are less transition at the logic circuit input than at the MUX input).

Page 3

Regarding claim 5, AAPA disclose, at least in Fig. 5, the first logic circuit operates according to a first truth table in the first mode and according to a second truth table in the second mode, and wherein the first truth table is not identical to the second truth table (see Fig. 2 and 3).

Regarding claim 6, AAPA disclose, at least in Fig. 5, 6. The system of claim 1, wherein the first logic circuit functions as an XOR gate (510) in the first mode.

Regarding claim 7, AAPA disclose, at least in Fig. 5, that the first logic circuit functions as an XNOR gate (output of 510 functions as an XNOR respect to the input signals B\_b and Ain) in the first mode.

Regarding claim 8, AAPA disclose, at least in Fig. 5, that the multiplexer is configured to invert (by 521) the logic circuit output signal when the first logic circuit is selected.

Regarding claim 9, AAPA disclose, at least in Fig. 5, that the multiplexer is configured to receive only 2 multiplexer input signals (xor\_out and C).

Regarding claim 10, AAPA disclose, at least in Fig. 5, that the multiplexer is configured to receive more than 2 multiplexer input signals (select line can be interpreted as input signal).

Method Claims 11, 13, and 15-20 are essentially the same in scope as apparatus claims 1, 3, and 5-10, and are rejected similarly.

## Allowable Subject Matter

Art Unit: 2819

Claims 2, 4, 12, and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

## Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel D. Chang Primary Examiner Art Unit 2819